DAC/µP-Supervisor Combination Improves Analog I/O Reliability

Using a DAC and microprocessor supervisor, the reliability of the analog I/O can be improved in systems employing an industrial controller, a programmable logic controller (PLC), or in a data acquisition system. A simple application is shown on how to implement this function. The analog output is set to zero when it detects a microprocessor failure or undervoltage condition without the need of an optocoupler.

The analog control signals used in industrial controllers, programmable-logic controllers (PLCs), and data-acquisition systems include 0-5V, 0-10V, ±5V, ±10V, and 4-to-20mA current loops. For safety reasons, some analog-output modules employ optocouplers to electrically isolate the microprocessor (µP) and analog circuits. Also for reliability and safety, other systems require that the analog outputs reset to midscale or zero in response to a µP failure.

These requirements are met by the circuit in the figure, which monitors µP activity and sets the analog output to zero when it detects a µP failure or undervoltage condition. It also improves the mean time before failure (MTBF) by minimizing I/O pins at the µP and by eliminating an optocoupler.
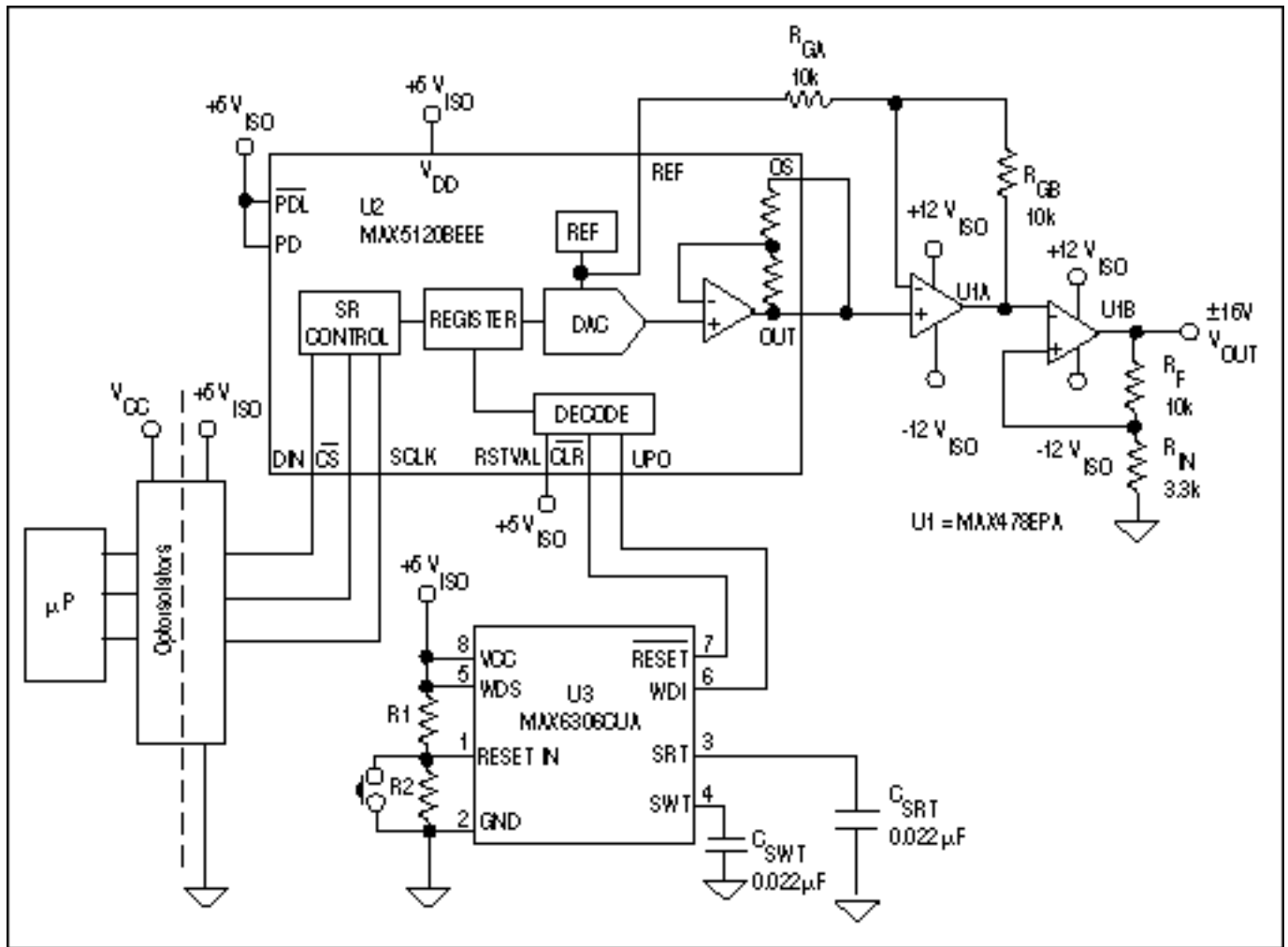
When a failure occurs in the supply voltage or µP operation, this DAC (U2) and µP supervisor (U3) together produce a user-programmed default output (V_{OUT}).

Three features enable the DAC (U2) to produce zero-scale resets: an asynchronous-reset input (CLR), a user-selectable reset-value input (RSTVAL), and a user-programmable output (UPO) for serial-interface setup. These built-in features also eliminate an optocoupler, minimize I/O pins at the µP, and lessen the need for external discrete circuitry. The µP supervisor (U1) includes a resistor-programmable reset-input threshold, a capacitor-programmable watchdog timer, and a reset-timeout period.

As DAC codes range from 000_{HEX} to FFF_{HEX}, the circuit output (V_{OUT}) ranges from -10V to +10V. Op amp U1A is offset by the DAC's internal, 10ppm/° C precision bandgap reference, and the output op amp (U1B) is configured as a buffer with a gain of four. Output voltage for the circuit is

$$VOUT = VREF \times (G \times NB/4096 - 1) \times (R_F/R_{IN} + 1),$$

where NB is the numeric value of the DAC's binary code, V_{REF} is the internal reference voltage, G is the gain of U1A, and R_F/R_{IN} is U1B's gain-resistor ratio.

U3 monitors the isolated supply voltage (V_{ISO}) via its V_{CC} pin. It also monitors µP activity via its WDI pin, and it generates a reset command via RESET. A resistor divider at RESET IN (pin 1) determines the reset-level threshold (V_{TH}). Similarly, the reset timeout period (t_{RP}) and watchdog timeout period (t_{WD}) are determined by capacitor values at SRT and SWT. Connecting WDS to VCC extends t_{RP} by a factor of 500. The following equations calculate values needed in the circuit:

$V_{RST} = V_{TH}(R1 + R2)/R2$, where $V_{TH} = 1.22V$ and V_{RST} is the adjustable reset threshold voltage.

$C_{RST} = t_{RP}/2.67$, where C_{RST} is in pF.

$C_{SWT} = t_{WD}/2.67$, where t_{WD} is in µs.

If V_{CC} fails, or if the µP locks up and cannot toggle WDI, U3 asserts low on its $\overline{RESET}$ output, which resets U2 via its CLR input. This action resets U2's output to the condition set by RSTVAL (to midscale in this case, which produces 0V at V_{OUT}). When U2 is being updated, its UPO output toggles U3's WDI at intervals less than the nominal watchdog timeout (t_{WD} = 25 seconds, subject to tolerances on the capacitor and the ICs). Other devices to consider for the watchdog function are the MAX6316 series and the MAX6369 series, which offer fixed timeout periods in SOT23 packages.

The switch between U3's RESET IN and GND terminals allows the user to command an emergency shutdown. $\overline{RESET}$ pulls CLR high after the reset timeout ($t_{RP} \cong 60ms$), but the DAC output remains at midscale until updated. The DAC's unipolar and bipolar modes allow it to produce all the common analog-output control signals.

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